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L14 same (control adj1 signal)	1

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L1	internal adj1 control adj1 signal	2371	L1

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L7: Entry 1 of 1 File: USPT Jun 1, 2004

DOCUMENT-IDENTIFIER: US 6744684 B2
TITLE: Semiconductor memory device with simple refresh control

Detailed Description Text (9):
Referring to FIG. 2, DRAM core MCR includes a memory array MB storing data, a row selection related circuit/command generation related circuit 16 responsive to, for example, 13-bit external address A0-A12 applied from high circuit complexity logic LG and external control signals exREADn and exWRITEn applied from high circuit complexity logic LG to generate an internal control signal specifying various operations, and providing a row related control signal such as a row predecoded signal, a column selection related circuit 14 receiving external addresses A0-A12 to generate a column related selection control signal, and a data input/output control circuit 20 transferring data between high circuit complexity logic LG and the memory array.

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L15: Entry 1 of 1 File: USPT Jun 8, 1999

DOCUMENT-IDENTIFIER: US 5910181 A
TITLE: Semiconductor integrated circuit device comprising synchronous DRAM core and logic circuit integrated into a single chip and method of testing the synchronous DRAM core

Abstract Text (1):
A semiconductor integrated circuit device includes a logic circuit and a synchronous dynamic random access memory including a core unit, integrated on a single semiconductor chip. The semiconductor integrated circuit device includes a synchronous dynamic random access memory control circuit which receives external control signals for the synchronous dynamic random access memory from the logic circuit, and outputs internal control signals to the core unit of the synchronous dynamic random access memory. For testing of semiconductor integrated circuit device, external test signals are provided through external terminals. The external test signals are selected by a selector, and are provided to the core unit of the synchronous dynamic random access memory for testing.

Brief Summary Text (29):
In another aspect of the present invention, the semiconductor integrated circuit device further comprises external input terminals for receiving and outputting internal control signals for the synchronous dynamic random access memory. A selector is provided for supplying internal control signals to the core unit of the synchronous dynamic random access memory. The internal control signals are obtained by selecting either first signals received from the external test input terminals or second signals received from the synchronous dynamic random access memory control circuit. The selector has a first mode for selecting the first signals received from the external test terminals, testing the semiconductor integrated circuit device directly, using the first signals. Further, the selector has a second mode for selecting second signals received from the synchronous dynamic random access memory control circuit.

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